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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

VO, TIM T

ART UNIT	PAPER NUMBER
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2112

DATE MAILED: 02/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/028,858

Applicant(s)

KAUSHIK ET AL.

Examiner

Tim T. Vo

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 04 February 2005.
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-10, 12-14 and 16-34 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) 1-10, 12-14 and 16-34 is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 12/19/01, 9/13/04
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____

Part III DETAILED ACTION

Notice to Applicant(s)

This application has been examined. Claims 1-10, 12-14 and 16-34 are pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1-10, 12-14 and 16-34 are rejected under 35 U.S.C. § 102(e) as being anticipated by Bealkowski et al. patent number 6,282,596 referred hereinafter "Bealkowski".

As for claims 1 and 8, Bealkowski teaches a method of adding one or more caching agents to a running computing device (see figure 1-3, hot plug processor cards 11, 20, 30 and column 3 lines 9-11, column 4 lines 4-11, wherein each processor card is hot plug and each processor card comprises a cache), comprising identifying the one or more caching agents provided by a hot plug module in response to the hot plug module being physically coupled to the running computing device (see figure 4 and column 7 line 51 to column 8 line 31, wherein each processor is identified with an agent ID and the hot plug controller uses the agent ID identify which processor card is removed or inserted to the computer system) ; and adding the identified caching agents of the hot

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plug module to a resource pool of the running computing device (see figure 2, service processor 31 and column 31-60, wherein the service processor 31 controls the hot plug controller and also monitoring the events in the computer such as insertion or removal and then stores such information to its own associated memory and controller routine); and enabling a communication interface of the hot plug module to establish a communication link with the running computing device (see figures 1-3, processor cards 11, 20, 30 are hot plugged to the data processing system 10 via the CPU connectors. Further, data processing system 10 supports hot plugging and initializing processor cards for communication between the newly added processor card and the processing system 10 via the CPU connectors as discloses in column 3 lines 1-15 and lines 35-41).

As for claims 2 and 9, Bealkowski further teaches comprising enabling a communication interface of the running computing device that is associated with the hot plug module in response to determining that the hot plug module has been physically coupled to the running computing device (see figure 4, wherein the flow chart describes the processor for establishing communication between the processor cards and the computer system).

As for claims 3 and 10, Bealkowski teaches performing a self test of the hot plug module, and in response to passing the self test, enabling the communication interface of the hot plug module to establish a communication link with the communication interface of the running computing device (see column 8 lines 31-39).

As for claim 4, Bealkowski teaches initializing the hot plug module, and after initializing the hot plug module, enabling the communication interface of the hot plug

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module to establish a communication link with the communication interface of the running computing device (see column 9 lines 10 lines 4-10).

As for claim 5, Bealkowski teaches wherein adding comprises adding one or more memory caching processors of the identified caching agents to a processor pool of the running system (see column 5 lines 53-60).

As for claim 6, Bealkowski teaches wherein adding comprises adding one or more memory caching input/output hubs of the identified caching agents to an input/output pool of the running system (see figure 1, CPU connector 14).

As for claim 7, Bealkowski teaches identifying memory of the hot plug module in response to the hot plug module being physically coupled to the running computing device; and adding the identified memory of the hot plug module to a memory pool of the running computing device (see column 8 lines 13-25).

As for claim 12, Bealkowski teaches in response to the hot plug removal request, providing an indication that a hot plug removal is in progress (see figure 5 and column 9 lines 33-51).

As for claim 13, Bealkowski teaches after removing the identified resources from the running computing device, providing an indication that the hot plug module may be removed; and disabling the communication interface of the running computing device to isolate the hot plug module from the running computing device (see figure 5 and column 9 lines 33-51).

As for claim 14, Bealkowski teaches a method of removing a hot plug module comprising one or more memory caches from a running computing device (see figure 1-

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3, hot plug processor cards 11, 20, 30 and column 3 lines 9-11, column 4 lines 4-11, wherein each processor card is hot plug and each processor card comprises a cache), comprising identifying resources of the hot plug module in response to a hot plug removal request (see figure 5 and column 9 lines 33-51); causing the hot plug module to write back modified cache lines of the one or more memory caches to the running computing device (see column 5 lines 53-60); and removing the identified resources from respective resource pools of the running computing device (see column 9 lines 33-51).

Bealkowski teaches waiting a predetermined time for pending transactions associated with hot plug module to complete; and disabling the communication interface of the running computing device to isolate the hot plug module from the running computing device after waiting the predetermined time (see figure 4, step 130 and column 9 lines 9-32).

As for claim 16, Bealkowski teaches readable medium for interrupt processing, comprising a plurality of instructions that in response to being executed result in a computing device in response to a hot plug interrupt examining a plurality of interface control registers associated with a plurality of communication interfaces for communicating with a plurality of hot plug modules having caching agents (see figure 4 and column 7 lines 51-65); and identifying which of a plurality of hot plug events caused the hot plug interrupt based upon the plurality of interface control registers (see column 8 lines 13-29).

As for claim 17, Bealkowski teaches, wherein the plurality of instructions in response to being executed further result in the computing device determining whether hot plug addition or hot plug removal has been requested for a hot plug module of the plurality of hot plug modules based upon an interface control register of the plurality of interface control registers that is associated with the hot plug module (see figures 4-5, wherein figure 4 discloses hot plug addition and figure 5 discloses hot plug removal).

As for claim 18, Bealkowski teaches, wherein the plurality of instructions in response to being executed further result in the computing device determining that hot plug removal has been requested for the hot plug module in response to the interface control register associated with the hot plug module indicating a pending hot plug interrupt and a joined state for the hot plug module (see figures 4-5, step 130 and column 9 lines 9-32).

As for claim 19, Bealkowski teaches, wherein the plurality of instructions in response to being executed further result in the computing device causing the hot plug module to write back modified cache lines to the running computing device; and removing resources of the hot plug module from the computing device (see column 5 lines 53-60).

As for claim 20, Bealkowski teaches, wherein the plurality of instructions in response to being executed further result in the computing device determining that hot plug removal has been requested for the hot plug module (see figure 5); waiting a predetermined time for pending transactions associated with hot plug module to complete (see figure 4, step 130 and column 9 lines 9-32); and disabling the

communication interface of the computing device to isolate the hot plug module from the computing device after waiting the predetermined time (see figure 5 step 146).

As for claim 21, Bealkowski teaches, wherein the plurality of instructions in response to being executed further result in the computing device determining that hot plug removal has been requested for the hot plug module (see figure 5); and disabling the communication interface of the computing device to isolate the hot plug module from the computing device after determining that all transactions associated with the hot plug module have completed (see figure 5 step 146).

As for claim 22, Bealkowski teaches, wherein the plurality of instructions in response to being executed further result in the computing device determining that hot plug addition has been requested for the hot plug module in response to the interface control register indicating that the associated communication interface is disabled, that a module is coupled to the associated communication interface, and that the associated communication interface is in a no module present state (see figure 4 and column 8 lines 1-6).

As for claim 23, Bealkowski teaches, wherein the plurality of instructions in response to being executed further result in the processor adding resources of the hot plug module to the running computing device in response to determining that hot plug addition has been requested for the hot plug module and that no other hot plug addition is in progress (see figure 4 and column 7 lines 51-65).

As for claim 24, Bealkowski teaches a hot plug module comprising a coupler for detachably coupling the hot plug module to a running computing device (see figure 1-3,

hot plug processor cards 11, 20, 30 and column 3 lines 9-11, column 4 lines 4-11, wherein each processor card is hot plug to the CPU connector 14); a communication interface to establish a communication link with the running computing device via the coupler in response to being enabled and to de-establish the communication link in response to being disabled (see figures 4-5, wherein figure 4 discloses enabling communication for addition of processor card and figure 5 discloses de-establish communication for removal of processor card); an interface control register associated with the communication interface to indicate and control whether the communication interface is enabled or disabled (see figure 2, hot plug controller 70), and a processor and associated memory cache, the processor to program the interface control register to enable and disable the communication interface based upon whether the hot plug module is ready to join the running computing device (see processor card 30, 20, 11 and figures 4-5 disclosing enable communication with added processor and figure 5 disclose disable communication with removed processor card).

As for claim 25, Bealkowski teaches wherein the processor writes back modified cache lines of the memory cache to the running computing device in response to hot plug removal being requested for the hot plug module (see column 5 lines 53-60).

As for claim 26, Bealkowski teaches, wherein the hot plug module comprises a status indicator that indicates a hot plug status for the hot plug module (see LED service indicator 72 and column 5 lines 41-52).

As for claim 27, Bealkowski teaches, wherein the processor performs a self test of the hot plug module in response to hot plug addition being requested for the hot plug

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module, and enables the communication interface in response to determining that the hot plug module passed the self test (see column 8 lines 31-56).

As for claim 28, Bealkowski teaches a computing device comprising, a midplane comprising a coupler and a hot plug interface to track a state associated with the coupler (see figure 1); a hot plug module comprising a coupler to detachably couple the hot plug module to the coupler of the midplane and resources coupled to the coupler of the hot plug module via a hot plug interface of the hot plug module (see figure 1, processor cards are connected to the CPU connectors 14 to the system bus 18), the hot plug module to update the state of the hot plug interface of the midplane to indicate when the resources are ready to join the computing device (see column 5 lines 41-52); and a processor coupled to the hot plug interface of the midplane (see figure 1, service processor 31), the processor to add the resources to the computing device without rebooting in response to determining that the hot plug interface of the midplane indicates the resources are ready to join (see column 1 lines 57-58).

As for claim 29, Bealkowski teaches, wherein the midplane comprises a hot plug monitor that provides the hot plug interface of the midplane with a signal indicative of whether the coupler of the hot plug module has been coupled to the coupler of the midplane, and the processor programs the hot plug interface of the midplane to generate a hot plug interrupt in response to a change in the signal that is indicative of whether the coupler of the hot plug module has been coupled to the coupler of the midplane (see column 8 lines 1-5).

As for claim 30, Bealkowski teaches, wherein the hot plug interface of the midplane detects whether framing packets are received from the hot plug interface of the hot plug module, and the processor programs the hot plug interface of the midplane to generate a hot plug interrupt in response to a change in receipt of framing packets (see column 7 line 52 to column 8 line 29).

As for claim 31, Bealkowski teaches a midplane of a computing device, comprising a plurality of couplers to detachably couple hot plug modules to the midplane (see figure 1, CPU connector 14); at least one switch to interconnect the plurality of couplers (see figure 3A, switch 82), the at least one switch comprising a plurality of communication interfaces to establish communication links with the hot plug modules that are coupled to the plurality of couplers (see figure 3A, switch 80 and column 7 lines 28-50), and a plurality of interface control registers to control the plurality of communication interfaces (see column 5 lines 53-60).

As for claim 32, Bealkowski teaches a system management processor to initialize hot plug modules coupled the plurality of couplers (see figure 2, service processor 31 and column 5 lines 30-60).

As for claim 33, Bealkowski teaches wherein the plurality of interface control registers track states of the plurality of communication interfaces and associated hot plug modules (see column 5 lines 30-60).

As for claim 34, Bealkowski teaches wherein the switch provides an indication as to when all pending transactions associated with a hot plug module to be removed have completed (see figure 4, step 130 and column 9 lines 9-32).

Response to Arguments

1. Applicant's arguments filed 11/30/04 have been fully considered but they are not persuasive.
2. In response to the applicant's arguments that Bealkowski fails to teach claims 1 and 24 enabling a communication interface of the processor cards 11a-11d. Figure 1, 3A-3B to Bealkowski clearly discloses the CPU connectors for the processor cards 11, 20 to plug into the data processing system 10. Further, Bealkowski teaches initialization routines between the processor cards 11, 20 and the data processing system 10 for establishing data communication, which disclosed in figure 4A-4B and column 3 lines 35-41).
3. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., claim 1 provides isolation at the hot plug module by requiring a communication interface of the hit plug (hot plug) module to establish a communication link with the running system.) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).
4. In response to the applicant's argument for claims 6, 8 that Bealkowski fails to teach memory caching input/output hubs. As for claim 6, Figure 1 to Bealkowski discloses processor cards are hot plugged to the CPU connectors and each processor card comprising L2 cache as discloses in column 2 lines 42-47. As for claims 7-10, figure 2 to Bealkowski teaches a service processor 31 and column 5 lines 31-60,

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wherein the service processor 31 controls the hot plug controller and also monitoring the events in the computer such as insertion or removal and then stores such information to its own associated memory and controller routine.

5. In response to the applicant's arguments that Bealkowski fails to teach waiting a predetermined time for pending transactions associated with hot plug module before disabling a communication interface in claim 14. Since the claim's language does not specify waiting a predetermined time means therefore examiner is broadly interprets waiting a predetermined time is equivalent to a delay process steps. Figure 5 to Bealkowski discloses a process for controlling the removal of hot plug processor card. Bealkowski clearly teaches **prior** to disconnecting a particular hot plug processor card there is a time delayed as discloses in steps 142, 144 to notify the OS to remove the processor card from operation. Step 146 clearly discloses **after** steps 142-144 for disabling the PWR_EN signal for the particular slot of the processor card to be removed. These teachings are equivalent to what is claimed.

6. In response to the applicant's arguments that Bealkowski fails to teach plurality of interface control registers in response to the hot plug event as claimed 16. Column 5 lines 31-60 to Bealkowski teaches a service processor 31 controls the hot plug controller and also monitoring the events in the computer such as insertion or removal and then stores such information to its own associated memory and controller routine.

7. In response to the applicant's arguments that Bealkowski fails to teach midplane having a hot plug interface and a hot plug module to update the state of the hot plug interface of the midplane to indicate when the resources are ready to join. Figure 1,

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front bus 18 (midplane) having the CPU connectors (hot plug interface) and processor cards 11, 20 (hot plug module) see figure 1 column 3 lines 9-15 and column 6 lines 18-21). Further, Bealkowski teaches the service processor 31 controls the hot plug controller and also monitoring the events in the computer such as insertion or removal and then stores such information to its own associated memory and controller routine as discloses in column 5 lines 31-60.

8. In response to the applicant's arguments that Bealkowski fails to teach a switch that comprises a plurality of interface control registers. Figure 3A to Bealkowski teaches the Power FET switches 82, 86 comprises clock buffer for controlling clock sources when a processor card is removed from the CPU connector (column 6 lines 46-53), Bealkowski also teaches the service processor 31 has its own associated memory for controlling routines such as initialization routines to enable communication for the hot plugged processor card (see column 3 lines 35-41) and recording hardware monitoring, logging events, and reporting on operating conditions within data system 10 (column 5 lines 53-60).

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within

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TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tim T. Vo whose telephone number is 571-272-3642. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Tim T. Vo
Primary Examiner
Art Unit 2112

2/4/05